Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.417”**

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**.559”**

**Top Material: Al**

**Backside Material: Ti/Ni/Ag**

**Bond Pad Size: G = .050” X .060” S = .050” X .323” min.**

**Backside Potential: DRAIN**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .417” X .559” DATE: 1/28/16**

**MFG: IXYS THICKNESS .008” P/N: IXFD32N100Q3**

**DG 10.1.2**

#### Rev B, 7/1